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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,350	08/19/2004	Johannes Petrus Maria Van Lammeren	NL02 0143 US	5975

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
09/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/505,350	VAN LAMMEREN, JOHANNES PETRUS MARIA	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's Request for continued examination filed 29 January 2007 has been received. Responsive to applicant's request, the claims filed 29 January 2007 have been entered and are considered below.

Specification

The specification is objected to because of the following informalities:

Headers such as "Background of the Invention", "Summary of the Invention", "Brief Description of the Drawings",... are needed throughout the specification. Appropriate correction is required.

Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "one or more

transistors" of each delay circuit and "each delay circuit driving more than one latch" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to claim 1, the instant application fails to disclose each delay circuit "comprising one or more transistors".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, there is no support found for the recitation of each delay circuit "comprising one or more transistors", therefore the above recitation is misdescriptive of the present invention.

Furthermore, the recitation of each delay circuit drives more than one latch is also misdescriptive. It can be seen in Fig. 4 that each delay τ drives only one latch. Furthermore, the recitation of "a small portion of the total number of switched during a cycle of a given signal are driven by the same delay circuit" seems to equate "the delay circuit" as either τ of Fig. 4 or B of Fig. 5. Thus, it can be seen that "the delay circuit" drives only one latch circuit of both Figs. 4 and 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Neudeck (USPN 5,701,335) in view of Josephson et al. (5,530,706) and in further view of Shizu (USPN 5,073,727).

With respect to claim 1, as far as understood, Neudeck discloses, "an integrate circuit (Fig. 1) comprising:

a plurality of pairs of latches (latches coupled between 138 and 140, i.e., every latch labeled 104 of Fig. 1 with latches 106, 110 and 108) being respectively clocked by two non-overlapping clock signal (CK and CKB); and

delay circuits (102, 112, 114, etc. that generate clocks CKN with CKNBN to CKNA to CKBNA, each circuit causes a delay see Col. 4 lines 12-15, i.e., one delay circuit consists of portion of 102, 112, 114, etc. that delays CK, other delay circuit consists of portion of circuits 102, 112, 114, etc. that delays CKB) are placed between clock-inputs of latches of a same clock signal (the delayed signals of CK drives latches 104, and the delayed clocks of CKB drives the latches of the second 104 after 138, 106, latch receiving 136, 108, and last latch 104 coupled to 140, each delay circuit is coupled

between CK and CKB and each above latch), wherein each delay circuit drives more than one latch (as can be seen above, each delay circuit drives more than one latch);

wherein a small portion of a total number of latches to be switched during a cycle of a given clock signal are driven by the same delay circuit (a small portion of latches between 138 and 112 are driven by 102, a small portion of latches are driven by 112, i.e., 106 and 104 driven by the CKN1 signal, and so forth until the output node of 140), thereby reducing substrate bounce (the reduction of substrate bounce is merely functional language, and since Neudeck circuit performs the above recited claim language it to reduces substrate bounce)."

Neudeck fails to specifically disclose the composition of the "delay circuits" (i.e., non-overlapping clock circuits 102, 112, 114, etc.). However, Neudeck discloses that the circuit of "Fig. 3 of U.S. application Ser. No. 08/539,382, Josephson et al.", now Josephson et al. (USPN 5,530,706), may be used to construct the circuits of 102, 112, 114, etc. (see Col. 3 lines 13-20). It would have been obvious to one of ordinary skill in the art at the time of the invention to construct the non-overlapping clock circuits 102, 112, 114, etc. with the circuit of Fig. 3 of Josephson et al., in order to have a simply constructed non-overlapping clock circuit as suggested by Neudeck.

While the above combination of Neudeck and Josephson et al. disclose non-overlapping clock generators (i.e., Fig. 3 of Josephson et al.) that are ostensibly composed of at least one transistor, the above combination fails to specifically disclose any of the logic circuits (i.e., NAND gates and inverters of Fig. 3 of Josephson et al.) being composed of at least one transistor. However, Shizu discloses in Fig. 4 a specific

inverter (i.e., circuit of Fig. 4) that is composed of three transistors and has reduced noise on its output signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the generic inverters of Fig. 3 of Josephson et al. with the specific inverters of Shizu for the purpose of reducing noise at the output of the inverters of the circuit of Fig. 3 of Josephson et al. thereby increasing the accuracy of the total combined circuit.

Response to Arguments

Applicant's arguments filed 29 January 2007 have been fully considered but they are not persuasive.

With respect to claim 1, Examiner disagrees with Applicant's arguments. The amended recitation is taught by the above combination as indicated in the above rejection of claim 1. Neudeck does, in fact, disclose a small portion of the total number of latches to be switched during a cycle of the clock signals CK and CKB are driven by the same delay. For example, the clock signals CK and CKB clock latches between 138 and 112 are delayed by 102, CKN1 and CKNB1 which are output by the delay of 112 clock the latches between 112 and signal lines 122 and 124, and so on to the output of 140. With respect to the limitation of each delay circuit "comprising one or more transistors", the instant application fails to disclose such a limitation, thus the above argument is not persuasive. The reduction of substrate bounce is merely the result/intended use of the invention, which cannot be relied upon to distinguish over

Neudeck (only structural or functional limitations in the claims are appropriate for defining over prior art). In any case, note that the circuitry of Neudeck is capable of reducing substrate bounce. Furthermore, it can be seen that the circuit of Fig. 1 of Neudeck is connected as recited in claim 1, and Neudeck operates as the recited circuit of claim 1.

The amendment does not overcome the previous rejection under 112 second paragraph as indicated in this and the previous office action. Applicant has failed to provide any arguments to indicate how the presently amended recitation adds any further clarification with respect to the rejection. Thus, this rejection is maintained.

Applicant has failed to file a replacement sheet indicating Fig. 1 and Fig. 2 as prior art or provide remarks responsive to the objection. Thus, this objection is maintained as well.

Applicant has failed to amend the specification responsive to the previous objection thereto with respect to not providing required headers and has failed to provide remarks responsive thereto. Thus, this objection is also maintained.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hazaucha et al. (USPN 6,798,248) discloses in Fig. 6, a circuit (300) that produces two complementary clock signals (CLKA, CLKB) that clock latch circuits (610) to prevent substrate bounce. Furthermore, Hazaucha et al. discloses in Fig. 8 that the complementary clock generator (300) of Fig. 6 may be replace with a complementary

clock generator (800) of Fig. 8 which generates multiple latching clocking signals based upon multiple delay circuits (t).

Takata (USPAPN 2003/0030472) and Makino (USPN 6,525,587) also disclose substrate bounce reducing circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

TH
September 6, 2007